What we claim is:

1. A packet processing device for processing a layered communication protocol comprising;

a receiving buffer of an upper layer,

a first means for notifying a free space of the receiving buffer,

a second means for reassembling a plurality of receiving packets into a single big packet based on the free space to be transmitted to the receiving buffer, and

a third means for determining a size of the big packet based on the free space.

2. The packet processing device as claimed in claim 1 wherein the first means is included in the upper layer and notifies the free space to the third means.

3. The packet processing device as claimed in claim 1 wherein the first means comprises a backward packet inclusive information reading circuit for detecting the free space based on information within a backward packet from the upper layer.

4. The packet processing device as claimed in claim 2 wherein the upper layer comprises a transport layer.

5. The packet processing device as claimed in claim 2 wherein the upper layer comprises an application layer and the big packet is transmitted not through a buffer of a transport layer but directly to the receiving buffer.

6. The packet processing device as claimed in claim 1, further comprising a connection identifying circuit for identifying a connection of the receiving packets,

the second means reassembling the big packet for each connection based on identification information of the identifying circuit.

7. The packet processing device as claimed in claim 1, further comprising a checksum calculating circuit for adding a checksum to the

big packet.

8. The packet processing device as claimed in claim 1 wherein the third means has a timer for giving the second means instructions for transmitting the big packet to the receiving buffer when a predetermined time elapses.

9. The packet processing device as claimed in claim 1 wherein the third means gives the second means instructions for assigning the big packet to the receiving buffer at a time when the big packet attains a size for issuance of an acknowledgement packet from the upper layer.

10. The packet processing device as claimed in claim 1 wherein the second means assembles the big packet with a first receiving packet including a header and subsequently received packets whose headers are deleted.

11. The packet processing device as claimed in claim 1, further comprising means for immediately transmitting the receiving packet to the receiving buffer without storing the receiving packet in the second means when the receiving packet is a non-accumulation packet.

12. The packet processing device as claimed in claim 1, further comprising an L3 switch which has a packet transfer function in a network layer made in a hardware form and transmits a plurality of receiving packets addressed to itself to the second means.

13. An NIC device comprising the packet processing device according to claim 1 for transmitting a plurality of receiving packets addressed to itself to the second means.